In the embodiments recited in claims 6 and 8, the element isolation regions are buried in a trench formed at a boundary between the element formation regions. In the embodiments recited in claim 7, the element isolation region isolates element formation regions formed of semiconductor layers formed on an insulation layer.

The examiner rejected claims 1-5 and 9-11 under 35 U.S.C. § 103(a) as obvious in light of a combination of the prior art devices shown in FIGS. 1-3 and U.S. Patent No. 5,856,215 (the "Jung patent"). Reconsideration is requested. Applicant respectfully submits that it is improper to combine the references as suggested by the Examiner.

FIG. 1 of the Jung patent shows a semiconductor device having two element formation regions separated by an element isolation region. The semiconductor device contains a pair of el-shaped gate electrodes. As appreciated by the examiner, the electrodes are not physically connected by a semiconductor layer. Therefore there is no possibility of the impurities migrating into a semiconductor layer. *A fortiori*, the Jung patent does not disclose or suggest a semiconductor device having first and second impurity storage regions, let alone a semiconductor device that includes a region that is effective for an impurity storage, while shortening the distance between the gate electrodes.

The Examiner urges that it would have been obvious to substitute the el-shaped electrode shown in the Jung patent for the prior art electrode shown in Fig. 2 of the instant application. However, the Examiner has the burden to show some teaching or suggestion *in the references* to support their use in the particular claimed combination. *SmithKline Diagnostics Inc. v. Helena Laboratories Corp.*, 8 USPQ2d 1468, 1475 (Fed. Cir. 1988). The absence of such a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 42 USPQ2d 1378, 1383 (Fed. Cir. 1997). The references relied upon by the Examiner provide no such suggestion or motivation. Applicant respectfully submits that the Examiner's assertion, "It would have been obvious to one of ordinary skill to change shape of gate electrode (sic) in order to achieve high density of CMOS on a wafer," at least as it applies to Applicants' claimed configuration, is based on impermissible hindsight. To draw on hindsight knowledge of the patented invention, when the prior art does not contain or suggest that knowledge, is to use the invention as a template for its own reconstruction -- an illogical and inappropriate process by which to determine patentability. *Sensonics Inc. v. Aerosonic Corp.*, 38

USPQ2d 1551, 1554 (Fed. Cir. 1996). Consequently, the rejection of pending claims 1,3-6 and 9-11 should be withdrawn.

The examiner rejected dependent claims 6-8 under 35 U.S.C. § 103(a) as obvious in light of a combination of the prior art devices shown in FIGS. 1-3, the Jung patent, and U.S. Patent No. 6,114,741 (the "Joyner *et al.* patent"). Reconsideration is respectfully requested. The Joyner *et al.* patent is cited merely because it teaches an element isolation region buried in a trench formed at a boundary between the element formation regions. However, nothing in any of these references would have suggested a semiconductor device having a pair of impurity storage regions physically connected by a semiconductor layer and arranged in a direction different from the direction of the arrangement of the gate electrodes. Therefore, the cited references would not have suggested the semiconductor devices recited in claims 6-8 and the rejection of these claims as obvious under 35 U.S.C. § 103(a) should be withdrawn.

CONCLUSION

In light of the foregoing amendments and remarks it is believed that the application is in condition for allowance so that a prompt and favorable response is earnestly solicited.

Respectfully submitted,

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June 5, 2001

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I hereby certify that this document and any fee being referred to as attached or enclosed is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, D.C. 20231, on

June 5, 2001 Kathleen Gaines
Date Kathleen Gaines

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claim 1 has been amended as follows:

1. (amended) A semiconductor device comprising:

a first element formation region in which a device of a first conductivity type is formed;

a second element formation region separated from said first element formation region by an element isolation region and in which a device of a second conductivity type different from said first conductivity type is formed;

a first gate electrode provided on said first element formation region and containing an impurity of the first conductivity type;

a second gate electrode provided on said second element formation region facing said first gate electrode and containing an impurity of the second conductivity type;

a first impurity storage region containing said first conductivity type impurity having one end connected to an end of said first gate electrode, and arranged in a direction different from the direction of arrangement of said first and second gate electrodes; and

a second impurity storage region, physically connected to said first impurity storage region by a semiconductor layer, said second impurity storage region containing said second conductivity type impurity, and having one end connected to an end of said second gate electrode, having the other end electrically connected to the other end of said first impurity storage region , and arranged in a direction different from the direction of arrangement of said first and second gate electrodes.

Claim 2 was canceled without prejudice.